Shanghai SVA - NEC Liquid Crystal Display Co., Ltd.

TFT COLOR LCD MODULE

(COMMON)

SVA260WX01SA

66cm (26.0 Type)

WXGA+

LVDS Interface （1 port）

DATA SHEET

(Version 1. 0)

Published by

Technology Department

SVA - NEC Liquid Crystal Display Co., Ltd.

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Confirmed by	***Date***

INTRODUCTION

• WARRANTY

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• HANDLING OF DOUBTFUL POINTS

Any question arising out of, or in connection with, this SPECIFICATION or any matter not stipulated herein will be settled each time upon consultation between both parties.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

SVA260WX01SA module is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATIONS

- Monitor for HDTV

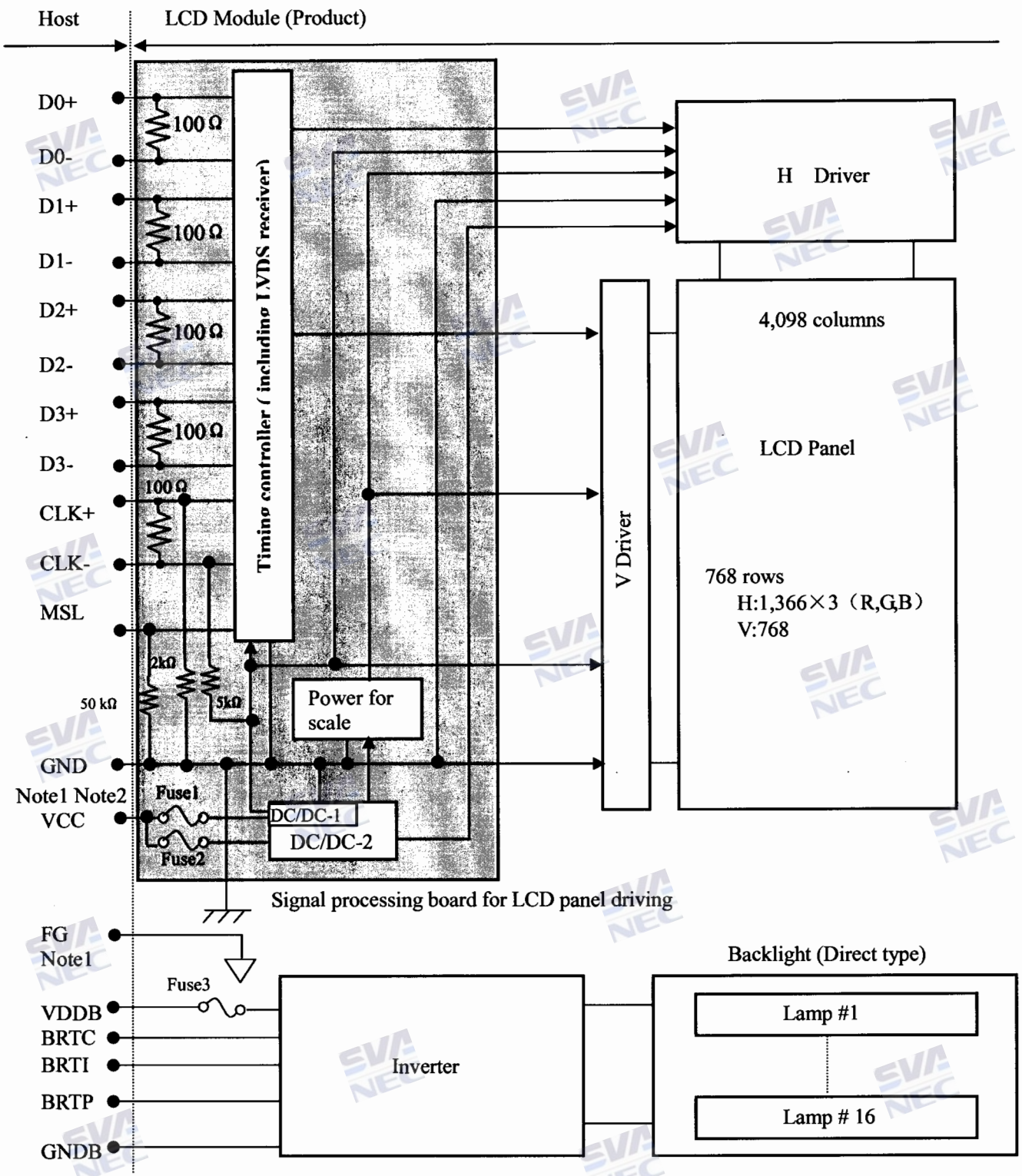
1.3 FEATURES

- a-Si TFT active matrix
- Resolution WXGA+ (1366×768 pixels)
- Luminance (500cd/m^2) (typ.)
- Contrast (550:1) (typ.)
- High gamut: 72% (typ.) ※against NTSC
- 8bit LVDS interface input
- 16.77 millions colors(8bit)
- Direct type backlight (with inverter)

2. GENERAL INFORMATION (under normal temperature)

Display area	575.77(H) x 323.71 (V) mm (typ.)
Display diagonal	66.0 cm (26.0 inches)
Drive system	a-Si TFT active matrix
Display color	16.77M colors (8bit)
Pixel	1,366 (H) ×768(V) pixels
Pixel arrangement	RGB (Red dot、Green dot、 Blue dot) vertical stripe
Dot pitch	0.1405(H)×0.4215(V) mm
Pixel pitch	0.4215(H)×0.4215(V) mm
Module size	626.0(typ., W) ×373.0(typ., H) ×48.0(max., D) mm
Weight	（4,300 g） (typ.)
Contrast ratio	550:1(typ.)
Viewing angle	Contrast ratio ≥ 10：1 • Horizontal: right 85° (typ.) , left 85° (typ.) • Vertical: up 85° (typ.) , down 85° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale (γ=2.2): normal axis
Polarizer surface treatment	Anti-glare (AG6)
Polarizer pencil hardness	3H (min.)
Color gamut	At LCD panel center 72 % (typ.) [against NTSC color space]
Response time	Ton + Toff (10%←→90%) 16 ms (typ.)
Luminance	At IBL = 5.0 mArms / lamp 500cd/m^2 (typ.)
Signal system	LVDS 1 port [RGB :8-bit, Dot clock (CLK), Data enable (DE)]
Power supply voltage	LCD panel signal processing board：5.0V LCD backlight : 24.0V
Backlight	Direct type：cold cathode fluorescent lamps. 16 piece pipes(with inverter) Replaceable part: Inverter board 260PW011S
Power consumption	Luminance to maximum and at sub pixel check (0/255) pattern 90 W (typ.)

3. BLOCK DIAGRAM



Note1: Inside the product, the connection of GND(System ground),FG(Frame ground) and VBLC(Lamp low voltage terminal), is being discussed.(GND-FG: not connected ,GND-VBLC: not connected ,FG-VBLC: not connected)

Note2: GND and FG should be connected with the custom equipment's Ground. Furthermore, it is recommended that GND,FG and inverter's Ground in the product should be connected together in customer equipment.

4. DETAILED SPECIFICATION

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	626.0± 1.0 (W) × 373.0± 1.0 (H) × 48.0 (max. , D) Note1,2	mm
Display area	575.77 (W) × 323.71 (H) Note1	mm
Weight	(4,300) (typ.)	g

Note: See "**7. MODULE OUTLINE**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	Signal processing board for LCD panel driving		VCC	(Vss-0.5 ~+6.5)	V	Ta = 25°C
	Backlight		VDDB	26.4	Vrms	
Backlight	Lamp current		IBL	7.0	mArms	
Input voltage for signals	Signal processing board for LCD panel driving (Note 1)		Vi	(-0.3~ +4.0)	V	Ta = 25°C VDD=5V
	Backlight inverter	(BRTC signals)	VBC	(-0.3~ +6.0)	V	Ta = 25 °C VDD=24V
		(BRTI signals)	VBI	(-0.3~ +6.0)	V	
		(BRTP signals)	VBP	(-0.3~ +6.0)	V	
Storage temperature			Tst	(-20 ~ +65)	°C	-
Operating temperature		Front surface	TopF	(0 ~ +55)	°C	Note2
		Rear surface	TopR	(0 ~ +65)	°C	Note3
Relative humidity Note4			RH	≤(90)	%	(Ta ≤40°C)
				≤(85)	%	(40°C<Ta≤50°C)
				≤(70)	%	(50°C <Ta≤55°C)
Absolute humidity Note5			AH	≤(73)	g/m3	(Ta > 55°C)
Operating altitude			-	≤(4，850)	m	(0°C<Ta≤50°C)
Storage altitude			-	≤(13，600)	m	(-20°C<Ta≤60°C)

Note1: Display signals are D0+/-, D1+/-, D2+/-, D3+/-, CK+/-， MSL
Note2: Measured at center of LCD panel surface (including self-heat)
Note3: Measured at center of LCD module's rear shield surface (including self-heat)
Note4: No condensation
Note5: The water content at Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta=25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VCC	(4.5)	5.0	(5.5)	V	-
Power supply current(Note1) max value(Note 2)		ICC	-	(770)	(1200)	mA	VCC=5.0V Fv=(60Hz) Fdclk=(75MHZ)
Permissible ripple voltage		VRP	-	-	(100)	mV	VCC
Differential input threshold voltage for LVDS receiver	Low	VTH	-	-	(+100)	mV	at VCM =(1.2V) Note3
	High	VTL	(-100)	-	-	mV	
Input voltage width for LVDS receiver		Vi	(0)	-	(2.4)	V	-
Terminal resistor		RT	-	100	-	Ω	-
Dot clock Oscillation frequency		Fdclk	(65)	(75)	(82)	MHz	-
Horizontal Oscillation frequency		fh	(44)	(47)	(53)	kHz	-
Vertical Oscillation frequency		fv	(48)	(60)	(66)	Hz	-
Rush current		Irush	-	-	(1.5)	A	-

Note1: Checked flag pattern
Note2:Sub pixel check pattern(0/255) for theoretical maximum current
Note3: Common mode voltage for LVDS driver

4.3.2 Driving for backlight lamp

(Ta=25°C) Note1

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current Note3	IBL	3.0	5.0	7.0	mArms	At IBL=5.0 mArms L=(500cd/m^2)
Lamp voltage Note2,Note3	VBLH	-	(860)	-	Vrms	-
Lamp starting voltage Note2,Note3,Note4	VS	-	-	(1,500)	Vrms	Ta = 25℃
		-	-	(1,650)	Vrms	Ta =0℃
Lamp oscillation frequency Note5	FO	55	60	65	kHz	-

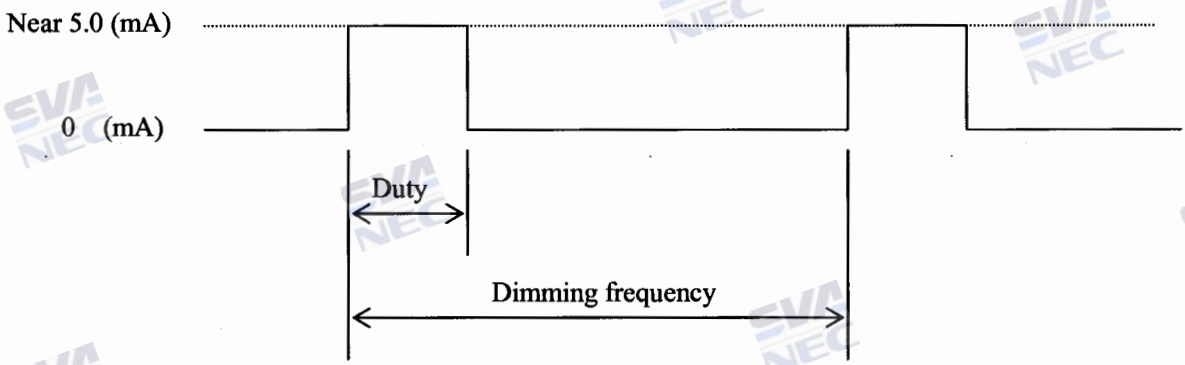
Note: The backlight of this product is made up of 16 piece lamp. The specification above is only for one lamp.

4.3.3 Backlight inverter

(Ta=25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage			VDDB	23.0	24.0	25.0	V	-
Power supply current *1			IDDB	3.15	3.5	3.9	mA	The maximum Luminance at VDDB=24.0V
Output current			IOmax	-	5.0	-	mArms	-
			IOmin	-	4.0	-	mArms	-
Open lamp voltage			VO	1650	-	-	V	-
Control system input voltage	(BRTC) Signal	High	VBCH	2.4	-	5.25	V	-
		Low	VBCL	0	-	0.8	V	
	(BRTI) Signal	-	VBI	0	-	3.3	V	-
	(BRTP) Signal	High	VBPH	2.4	-	5.25	V	-
		Low	VBPL	0	-	0.8	V	-
Control system input current	(BRTC) Signal	High	IBCH	-	-	1000	μA	-
		Low	IBCL	-1000	-	-	μA	-
	(BRTI) Signal	-	IBI	-1000	-	1000	μA	-
	(BRTP) Signal	High	IBPH	-	-	3500	μA	-
		Low	IBPL	-1580	-	-	μA	-

*1 The waveform of the current flowing into the inverter is as follows:



Duty: dimming to maximum 100% ~ dimming to minimum 20%, dimming frequency: (180) Hz (TYP.)

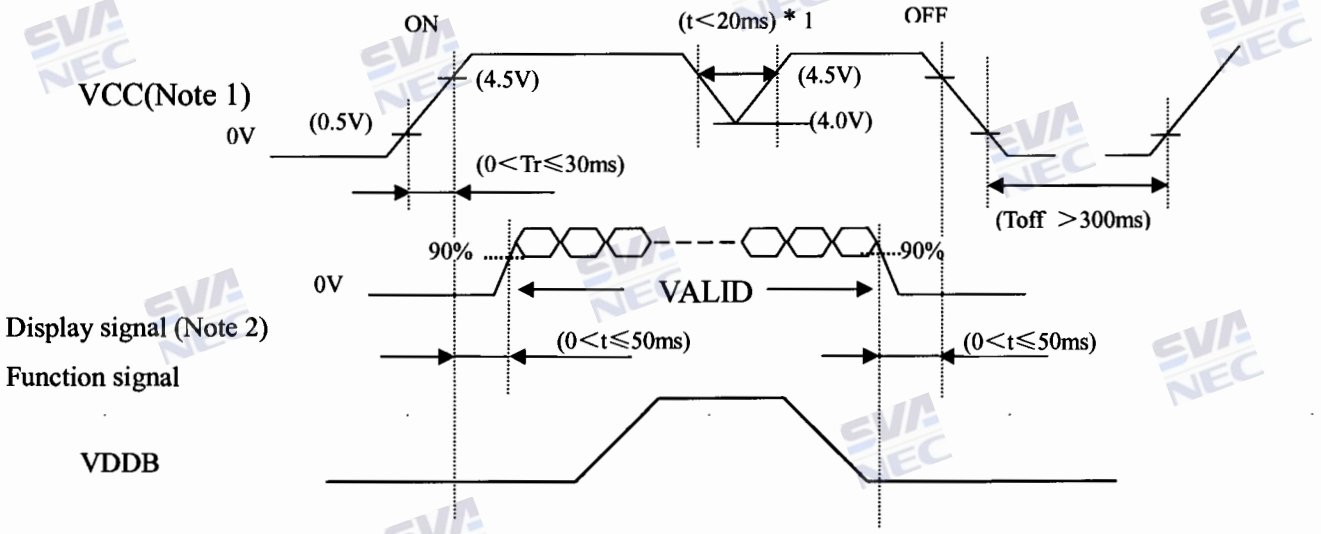
Note 1: In case the outer pulse dimming is selected, see "**4.6.2 detailed PWM dimming timing**"

Note 2: During light dimming, big ripple voltage occurs in the power supply line. Ripple voltage will cause audio noise and signal waveform noise in the system circuit (such as audio circuit) to occur.

In case the noise in the system circuit has occurred, electrolytic capacitor of several kilo μF should be assembled between the power lines(VDDB and GNDB).Then the noise can be reduced.

4.4 POWER SUPPLY VOLTAGE SEQUENCE AND RIPPLE

4.4.1 Power supply voltage and B/L control sequence



※: The signal line is not connected with the module, at the end of cable the terminal resistor of 100Ω should be added.

Note 1: In terms of voltage variation (voltage drop) while VCC rising edge is below 4.5V, a protection circuit may work, and then this product may not work.

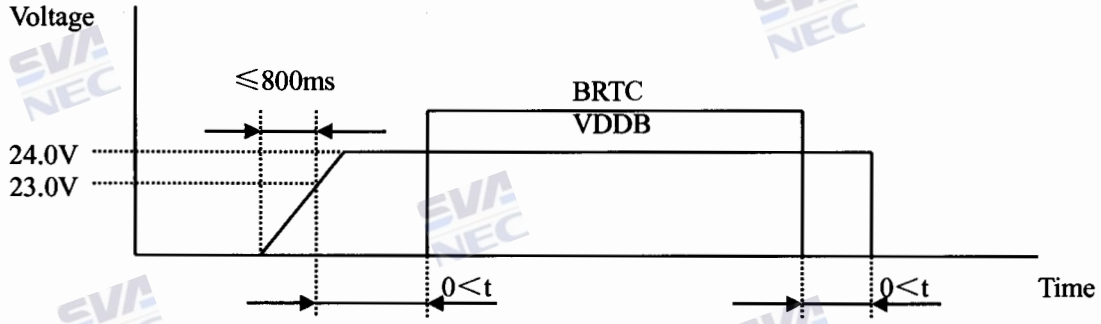
Note2: In order not to damage the inner circuit, display signals (D0+/-, D1+/-, D2+/-, D3+/- and CK+/-)must apply low or high impedance, exclude the VALID period (See above sequence diagram).

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should cut VCC.

Note3: When VDD is on, it should be set above 4.5V.

Note4: The backlight power supply voltage should be inputted within the valid period of display and function signals, in order to avoid unstable data display.

4.4.2 Backlight timing



Note1: In order to prevent unstable data displaying, inverter's power supply voltage should be input in the valid period of LVDS signals.

Note2:If the time for VDDB to start up is over 800ms,inverter's protection circuit will work, and then backlight will not be on.

4.4.3 Power supply voltage ripple

When the power supply is designed, the next form can give the reference. If the voltage ripple is over the value in next form, the noise should be seen in display area.

Ripple (Measured at input terminal of power supply)

Parameter	Power supply voltage	Permissible ripple voltage Note 1 (Measured at input terminal of power supply)	Unit
VCC	5.0V	(≤100)	mVp-p
VDDB	24.0V	(≤200)	mVp-p

Note 1: Permissible ripple voltage contained spike noise.

4.4.4 Fuse

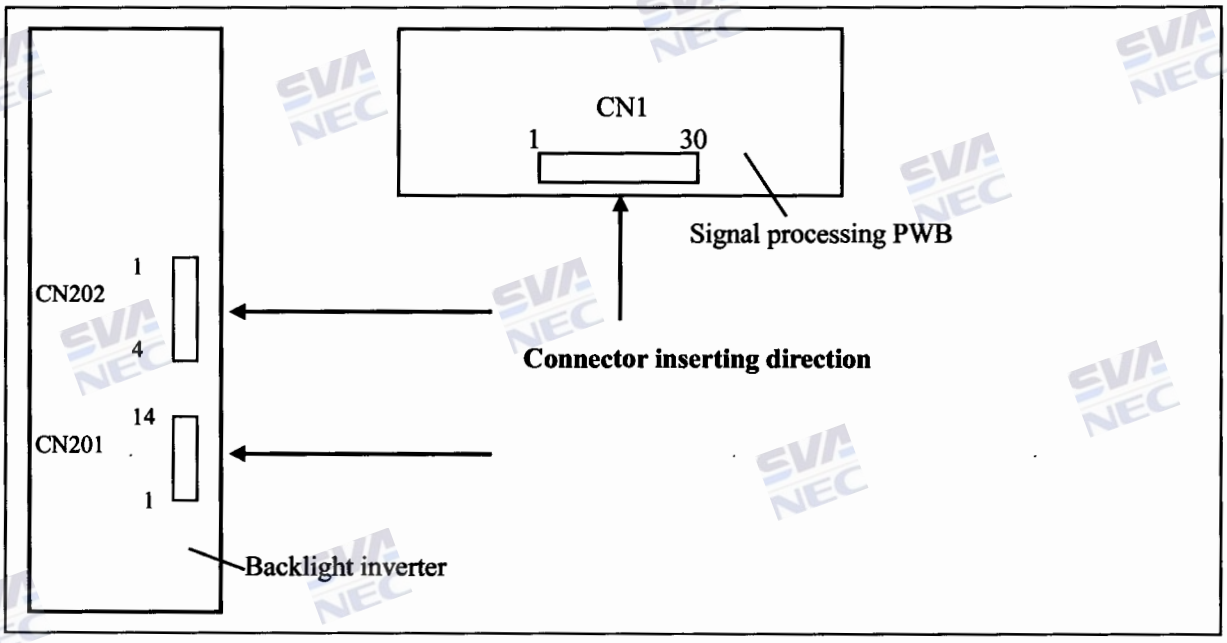
Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
Fuse1(VCC)	FCC16202AB	Kamaya electric Co.Ltd	2.0A 32V	5A（~5second）	Note 1
Fuse2(VCC)	FHC16322AD	Kamaya electric Co.Ltd	3.15A 24V	7.875A（~5second）	
Fuse3(VDDB)	25H6300G	SkyGate Co.,Ltd Japan	6.3A 125V	12.6A（~60second）	

Note1: The power supply capacity should be above the fusing current. . If the power supply capacity is less than the fusing current, the fuse may blow in a short time, and then nasty smell, smoking and so on may occur.

4.5 INTERFACE AND CONNECTOR PIN ALIGNMENT

4.5.1 Connectors for power supply and signals

The rear side of the product



Note 1: Connector's position is not given to correct position as the above drawing shows.
Note 2: Board's size and shape showed in the above drawing are not the same as the correct image drawings.

CN1: FI-E30S (Produced by JAE) Adaptable connector: FI-E30C (Produced by JAE)

Pin No.	Symbol	Signal	Function	
1	N.C	-	Keep open	
2	N.C	-	Keep open	
3	N.C	-	Keep open	
4	GND	Ground	Connect with the system GND	
5	D0-	Pixel data	Pixel data input(LVDS level)	
6	D0+			
7	GND	Ground	Connect with the system GND	
8	D1-	Pixel data	Pixel data input(LVDS level)	
9	D1+			
10	GND	Ground	Connect with the system GND	
11	D2-	Pixel data	Pixel data input(LVDS level)	
12	D2+			
13	GND	Ground	Connect with the system GND	
14	CLK-	Pixel clock	Pixel data's clock input(LVDS level)	
15	CLK+			
16	GND	Ground	Connect with the system GND	
17	D3-	Pixel data	Pixel data input(LVDS level)	
18	D3+			
19	GND	Ground	Connect with the system GND	
20	N.C	-	Keep open	
21	MSL	LVDS input MAP select terminal	High(3.3V)	Input map B mode
			Low(GND) or Open(N.C)	Input map A mode
22	N.C	-	Keep open	
23	GND	Ground	Connect with the system GND	
24	GND			
25	GND			
26	VCC	5.0V DC power	5.0V was supplied	
27	VCC			
28	VCC			
29	VCC			
30	VCC			

Note1: The ports of VCC and GND should be all used. As for the input of LVDS, please use the twisted pair wire of the transmission impedance 100Ω.

Note2: System ground (GND), Frame ground in the product should be connected together in customer equipment.

4.5.2 Connector for backlight

CN201: (S14B-PH-SM3(JST)) <Adaptable socket : (PHR-14(JST)>

Pin NO.	Symbol	Function		
1	VDDB	Power supply voltage 24.0V for backlight		
2	VDDB			
3	VDDB			
4	VDDB			
5	VDDB			
6	GNDB	Power's ground for backlight		
7	GNDB			
8	GNDB			
9	GNDB			
10	GNDB			
11	N.C	Keep open		
12	BRTC	Backlight ON/OFF alteration signal	High or Open	Backlight on
			Low	Backlight off
13	BRTI	Adjustable voltage dimming signal (0~3.3V)		
14	BRTP	PWM dimming signal		

CN202: B4B-ZR-SM3 (JST) <Adaptable socket: (ZHR-4(JST)>

Pin NO.	Symbol	Function		
1	BRTP	PWM dimming signal		
2	BRTI	Adjustable voltage dimming signal (0~3.3V)		
3	BRTC	Backlight ON/OFF alteration signal	High or Open	Backlight on
			Low	Backlight off
4	GNDB	Power ground for backlight		

4.6 Dimming control

4.6.1 Dimming control method

<table>
<tr><th>Mode</th><th>Dimming method and luminance ratio</th><th>BRTP signal</th></tr>
<tr><td>Voltage adjustable mode
Note 1</td><td>• Dimming method
When BRTI signal is input between BRTI and GNDB, no-step luminance tune can be done.
Furthermore, in case BRTI terminal is open, luminance maximum can reach.
• Luminance ratio Note 3
<table><tr><th>BRTI signal (VBI)</th><th>Luminance ratio</th></tr><tr><td>0 V</td><td>20%(min.)</td></tr><tr><td>3.3V</td><td>100%(max.)</td></tr></table></td><td>Open</td></tr>
<tr><td>Pulse width modulation mode
Note 1
Note 2</td><td>• Dimming method
If pulse width modulation(PWM) signals (BRTP signal) are input to BRTP terminal ,PWM dimming mode will work. Luminance is modulated according to the duty ratio of BRTP signal.
• Luminance ratio Note 3
<table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>0.2</td><td>20%(min.)</td></tr><tr><td>1.0</td><td>100%(max.)</td></tr></table></td><td>PWM signals</td></tr>
</table>

Note 1: At voltage adjustable mode, according to LCD panel signal processing board's input signal timing, display noise may occur.
In case interferential noise occurred in the display image, PWM method should be used.

Note 2: Refer to "**4.6.2 detailed PWM dimming timing**"

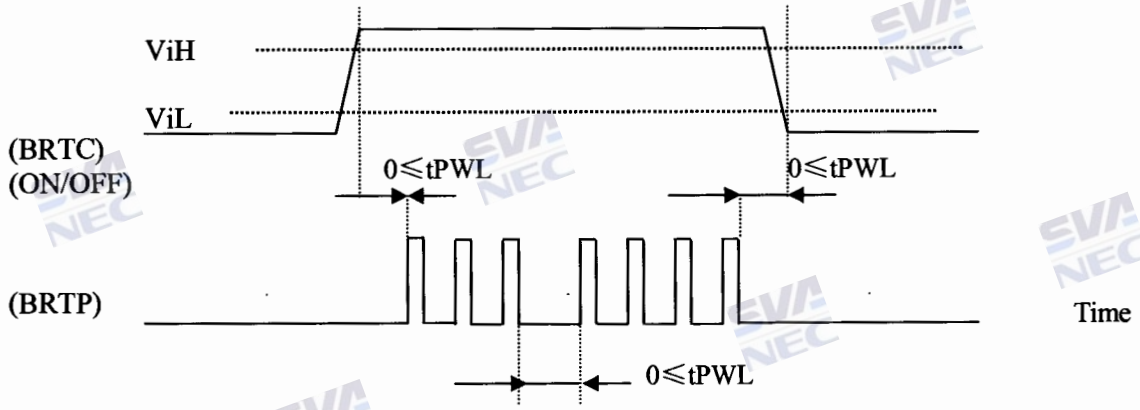
Note 3: The data in the sheet is reference value.

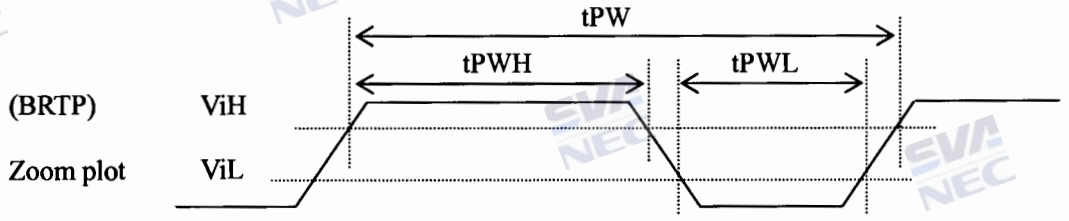
4.6.2 Detailed PWM dimming timing

From BRTP terminal, outer pulse is input to get into dimming. Dimming depends on pulse's duty ratio, at 100% (H range) luminance reaches maximum, at 20% reaches minimum.

- When BRTP="LOW" or "Open" ,BRTI will get valid.
- When voltage is added to the BRTP terminal, VDDB and BRTC should be on.

Outer pulse AC timing





	Symbol	Min	Typ	Max	Unit	Remarks
PWM Frequency	1/tPW	120	-	240	Hz	-
PWM Duty ratio	tPWH/ tPW	20	-	100	%	Luminance to maximum at 100%
Input voltage	ViL	0	-	0.8	V	-
	ViH	2.4	-	5.25	V	-

The setting of frequency should refer to the following formula:

Setting frequency =Vsync Frequency × （n+0.25）or (n+0.75)

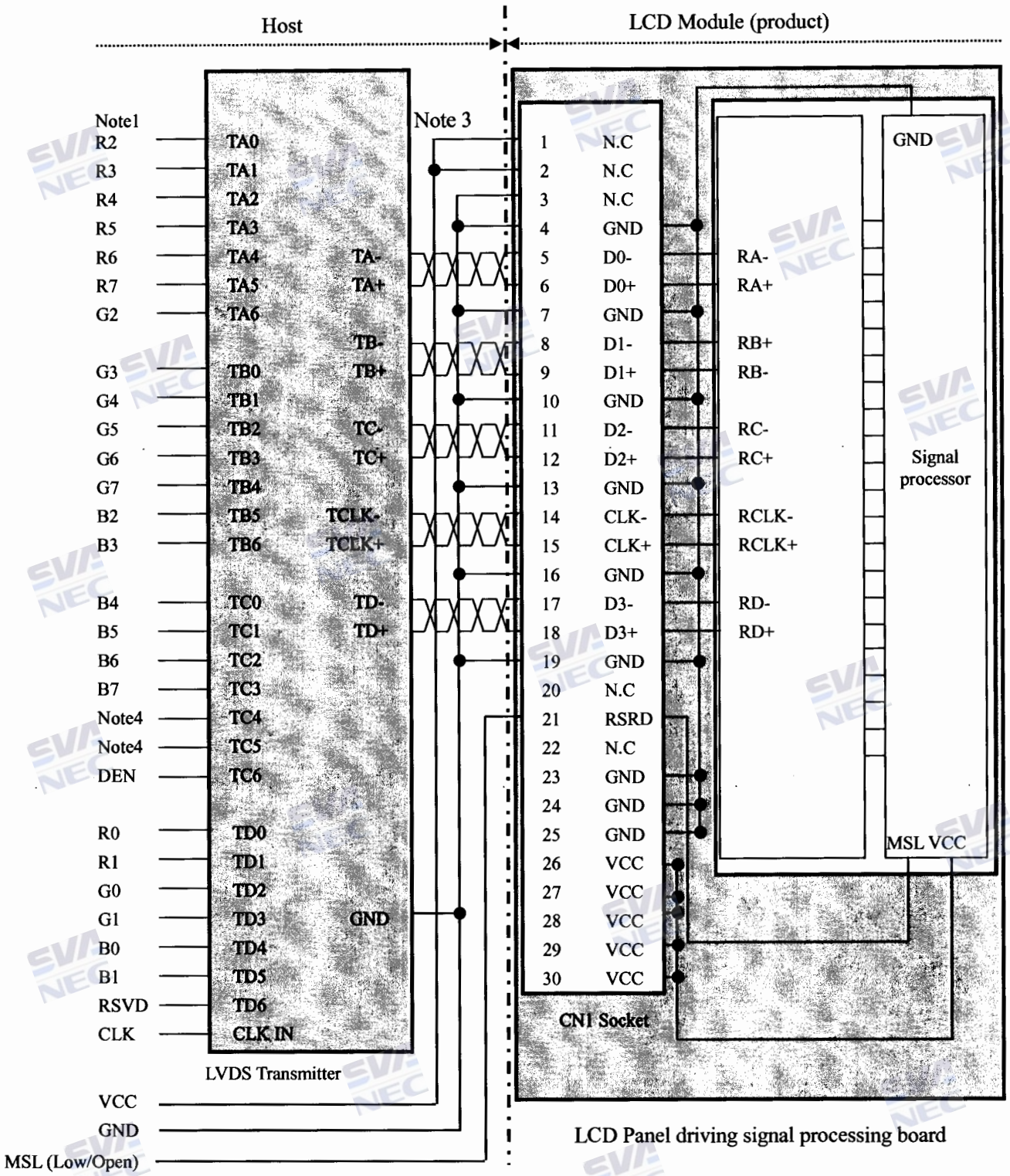
At setting frequency, because outer pulse input dimming interferes with inner signal frequency, display quality will become inferior. This condition should be fully estimated.

4.7 LVDS INPUT I/F MAP

This product uses CN1 21 pin (Terminal name: MSL), the following two modes of LVDS input map can be selected.

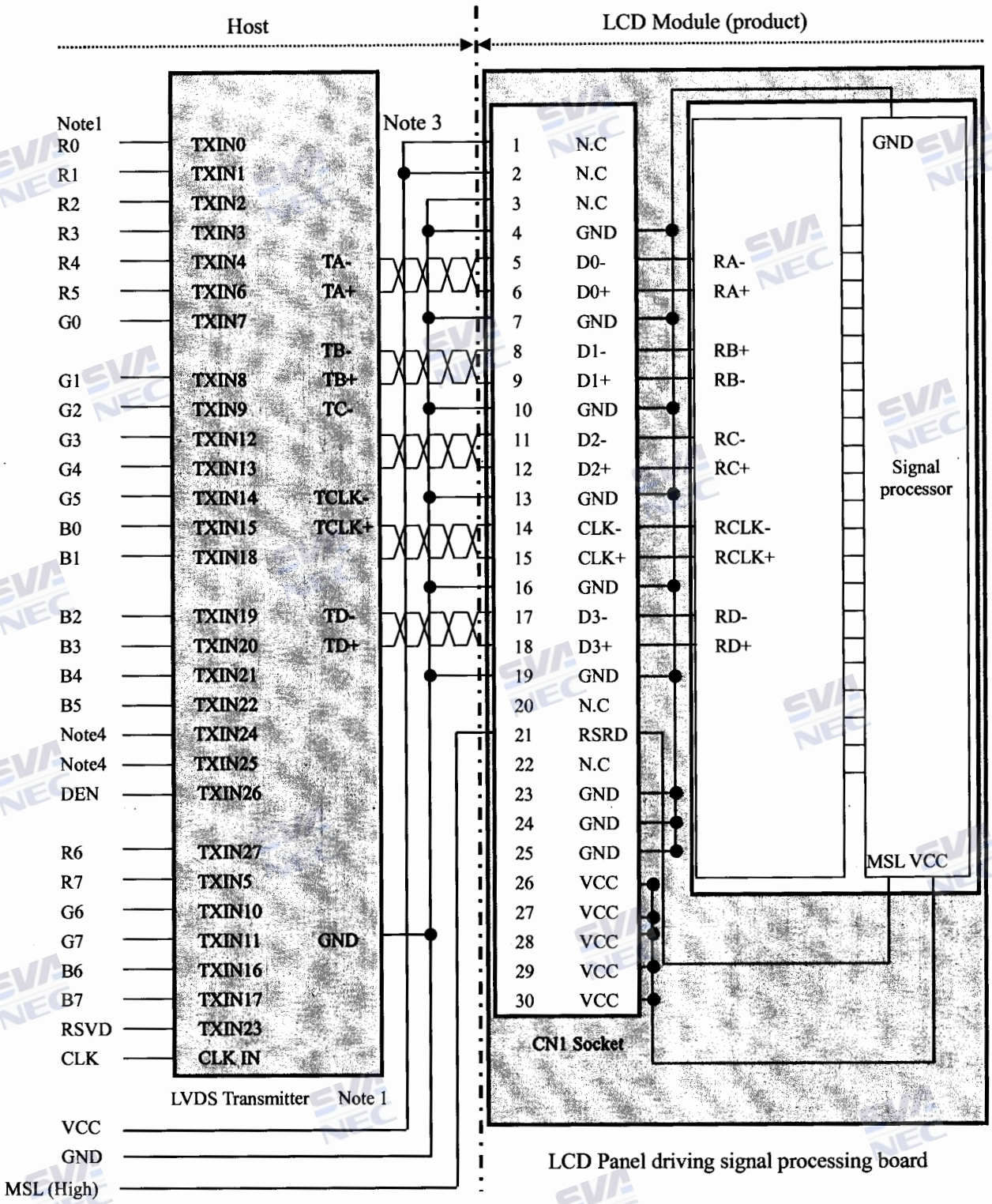
Pin No.	Symbol	Signal name	Function
21	MSL	LVDS input MAP select	Input MAP alternate(TTL level) "H" : Input map B mode "L or Open": Input map A mode

4.7.1 LVDS input map A (MSL: Low(GND) or Open(N.C))



Note 1: LSB(the least significant bit) -R0,G0,B0 MSB(the most significant bit) -R7,G7,B7
Note2: As for the input of LVDS, please use the twisted pair wire of the transmission impedance 100Ω.
Note3: Though the input signals to TC4, TC5 are not used in the product, please don't open them to avoid the noise's influence.

4.7.1 LVDS input map B(MSL: High(3.3V))



Note 1: LSB(the least significant bit) -R0,G0,B0 MSB(the most significant bit) -R7,G7,B7
Note 2: As for the input of LVDS, please use the twisted pair wire of the transmission impedance 100Ω.
Note 3: Though the input signals to TXIN24,TXIN25 are not used in the product, please don't open them to avoid the noise's influence

4.8 DISPLAY COLORS AND INPUT DATA SIGNALS

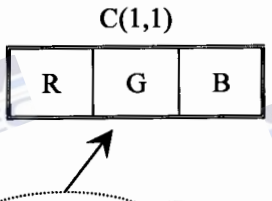
This product can display in equivalent to 16,777,216 colors in 256 scales. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal（0:Low level 、1:High Level）																							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:								:								:				
	↓				:								:								:				
	Bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑				:								:								:				
	↓				:								:								:				
	Bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:								:								:				
	↓				:								:								:				
	Bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note: Combination with 8 bit(256 grayscale) R,G,B color signal , the color can be formed.

4.9 DISPLAY POSITION

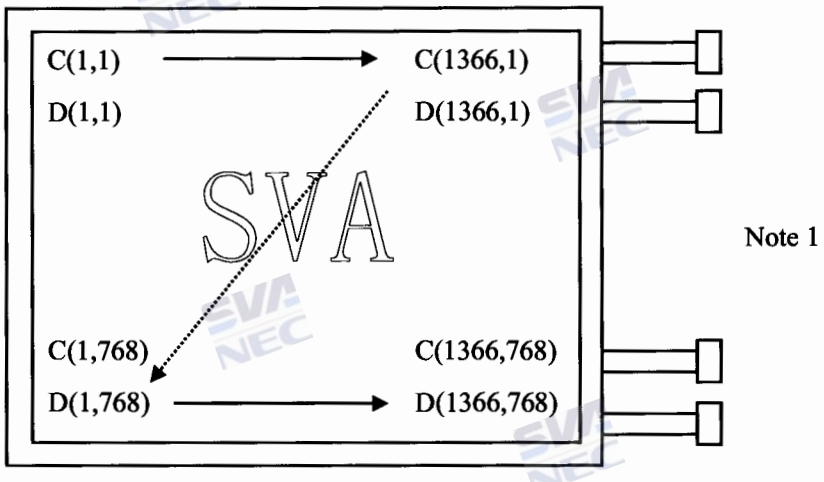
The following chart is the coordinates of per pixel l(See **"4.10 SCANNING DIRECTION".**).



C(1,1)	C(2,1)	• • •	C(X,1)	• • •	C(1365,1)	C(1366,1)
C(1,2)	C(2,2)	• • •	C(X,2)	• • •	C(1365,2)	C(1366,2)
•	•	•	•	• • •	•	•
•	•	• • •	•	• • •	•	• • •
•	•	•	•	• • •	•	•
C(1,Y)	C(2,Y)	• • •	C(X,Y)	• • •	C(1365,Y)	C(1366,Y)
•	•	•	•	• • •	•	•
•	•	• • •	•	• • •	•	• • •
•	•	•	•	• • •	•	•
C(1,767)	C(2,767)	• • •	C(X,767)	• • •	C(1365,767)	C(1366,767)
C(1,768)	C(2,768)	• • •	C(X,768)	• • •	C(1365,768)	C(1366,768)

4.10 SCANNING DIRECTION

The following figures are seen from a front view. Also the arrow shows the direction of scan.



Note1: Meaning of C(X,Y) and D(X,Y)

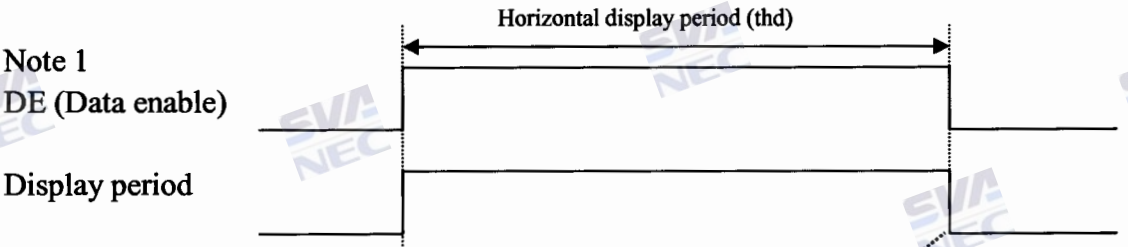
C(X,Y): The coordinates of the display position(See**"4.9 DISPLAY POSITION".**)

D(X,Y): The data number of input signal for LCD panel signal processing board.

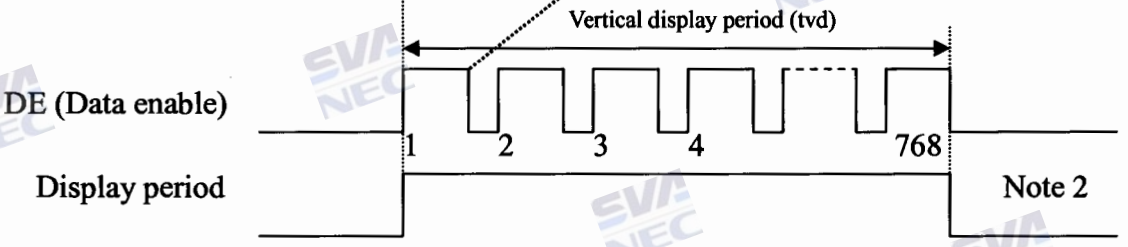
4.11 INPUT SIGNAL TIMINGS FOR LCD PANEL SIGNAL PROCESSING BOARD

4.11.1 Outline of input signal timings

• Horizontal signal



• Vertical signal Note 1



Note1: This diagram indicates virtual signal for set up to timing.
Note2: Pulse number (see"**4.11.3 INPUT TIMING CHART**")

4.11.2 Timing specification

(Note1)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	DOT frequency		1/tc	(65.0)	(75.0)	(82.0)	MHz	(13.333ns) (typ.)
	Horizontal frequency		Fh	(44.0)	(47.0)	(53.0)	kHz	
	Vertical frequency		Fv	(48.0)	(56.0)	(66.0)	Hz	(16.666ms) (typ.)
	Duty		—	—			—	Note2
	Rise time, Fall time		—				ns	
DATA	CLK-DATA	Setup time	—	—			ns	Note2
		Hold time	—				ns	
	Rise time, Fall time		—				ns	
DE	Horizontal	Cycle	th	(17.976)	(21.333)	—	μs	(46.875KHz)(typ.)
				(1,474)	(1,600)	(2,000)	CLK	Note3
		Display period	thd	1,366			CLK	—
	Vertical (One frame)	Cycle	tv	-	(16.666)	(18.182)	ms	(55.937Hz) (typ.)
				(773)	(838)	(1024)	H	
		Display period	tvd	768			H	
	CLK-DE	Setup time	—	—			ns	Note2
		Hold time	—				ns	
	Rise time, Fall time		—				ns	

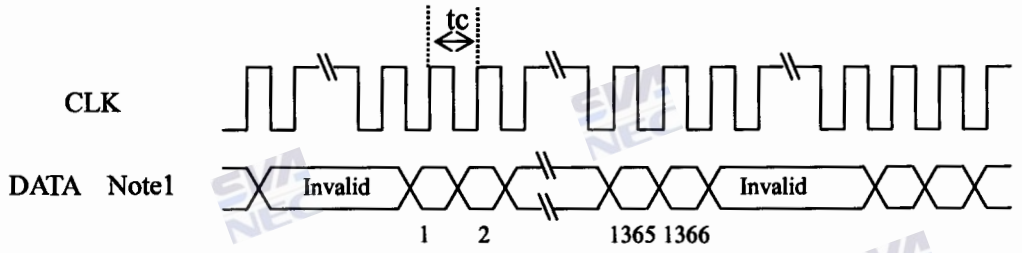
Note1: Definition of parameters is as follows.
tc=1CLK,Th=1H,Vf=1/tv

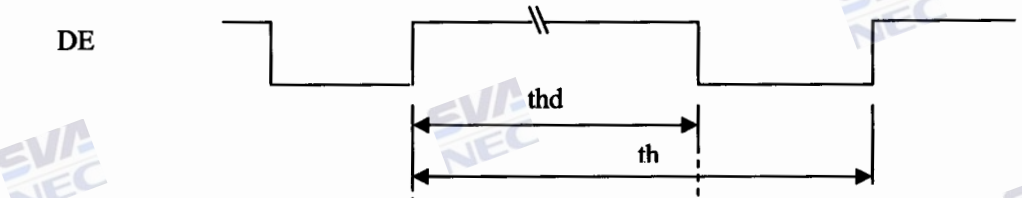
Note2: See the data sheet of LVDS transmitter.

Note3: "th" must keep the fluctuation within ±1 CLK, because of avoidance of image sticking.

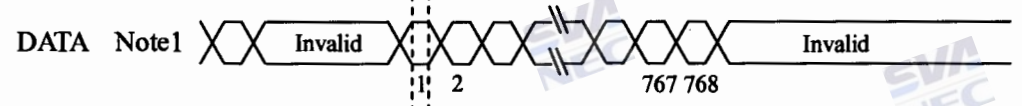
4.11.3 INPUT TIMING CHART

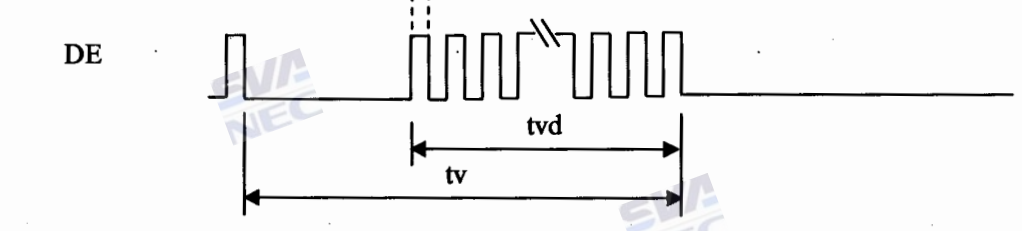
Horizontal timing





Vertical timing





Note 1: DATA=R0-R7, G0-G7, B0-B7

4.12 OPTICS

4.12.1 Optical characteristics

Note1 ,Note2

Parameter Note1		Condition	Symbol	min.	typ.	max.	Unit	Remarks
Luminance		White at center θR=0°, θL=0°, θU=0°, θD=0°	L	TBD	500	-	cd/ m^2	-
Contrast ratio		White/Black at center θR=0°, θL=0°, θU=0°, θD=0°	CR	TBD	550	-	-	Note3
Luminance uniformity		White θR=0°, θL=0°, θU=0°, θD=0	LU	-	(1.2)	(1.3)	-	Note4
Chromaticity	White	X coordinate(reference value)	Wx	(0.242)	(0.272)	(0.302)	-	Note5
		Y coordinate(reference value)	Wy	(0.247)	(0.277)	(0.307)	-	
	Red	X coordinate(reference value)	Rx	-	(0.643)	-	-	
		Y coordinate(reference value)	Ry	-	(0.332)	-		
	Green	X coordinate(reference value)	Gx	-	(0.270)	-		
		Y coordinate(reference value)	Gy	-	(0.587)	-		
	Blue	X coordinate(reference value)	Bx	-	(0.143)	-		
		Y coordinate(reference value)	By	-	(0.063)	-		
Color gamut		θR=0°, θL=0°, θU=0°, θD=0 At center,against NTSC	C	(65)	72	-	%	
Response time		black to White	Ton	-	7	TBD	ms	Note6 Note7
		white to Black	Toff	-	9	TBD	ms	
		Ton+Toff	-	-	16	TBD	ms	
		G TO G	Tg	-	8	TBD	ms	
Viewing angle	Right	θU=0°, θD=0°,CR≥10：1	θR	(70)	85	-	°	Note8
	Left	θU=0°, θD=0°,CR≥10：1	θL	(70)	85	-	°	
	Up	θR=0°, θL=0°,CR≥10：1	θU	(70)	85	-	°	
	Down	θR=0°, θL=0°,CR≥10：1	θD	(70)	85	-	°	

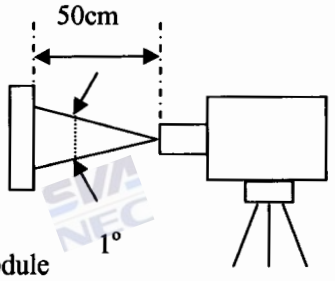
Note1: The values in upper table are only initial characteristics.

Note2: Measurement conditions are as follows.

Ta=25°C，VCC=5.0V，VDDB=24.0V，dimming to maximum.

Display mode：WXGA+，Horizontal cycle=1/46.875KHz，Vertical cycle=1/60.000Hz

Optical characteristics are measured at luminance saturation after 20minutes from working the product in the dark room. Also measurement method for luminance is as follows.



Luminance Meter (TOPCON BM-5A)

Spectroradiometer(TOPCON SR-3)

Note 3: See**"4.12.2 Definition of contrast ratio".**

Note 4: See**"4.12.3 Definition of luminance uniformity".**

Note 5: CIE 1931 Chromaticity Diagram Standard.

Note 6: Product surface temperature： TopF = (35) ℃

Note 7: See **"4.12.4 Definition of response times".**

Note 8: See **"4.12.5 Definition of viewing angles".**

4.12.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

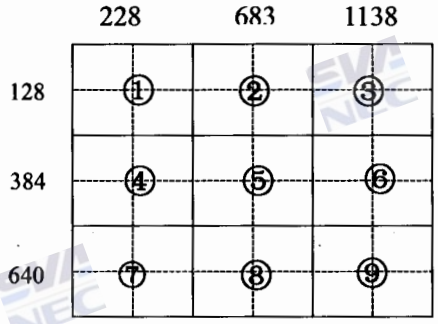
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.12.3 Definition of luminance uniformity

The luminance uniformity is calculated by using the following formula.

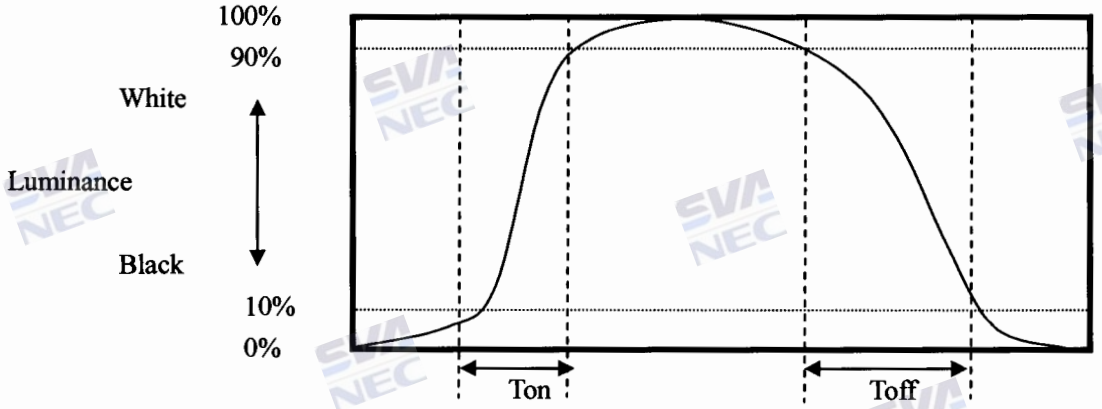
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑨}}{\text{Minimum luminance from ① to ⑨}}$$

The luminance is measured at near the 9 points shown below.

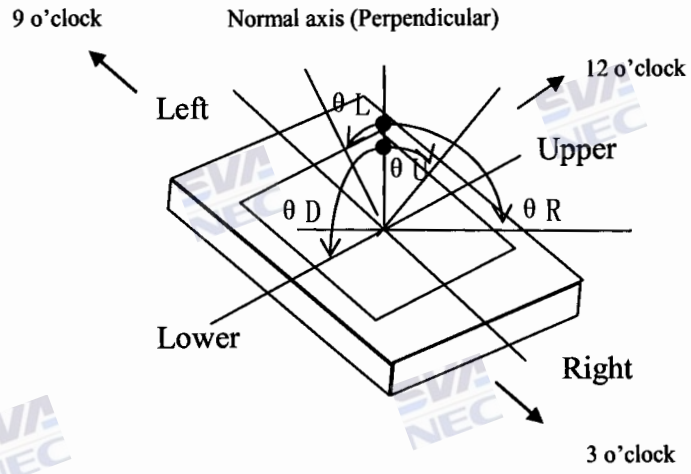


4.12.4 Definition of response times

Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10%. (See the following diagram.)



4.12.5 Definition of viewing angle



4.13 DEFECT CRITERIA

4.13.1 Display specification

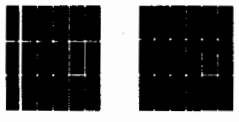
(Note1, Note 2)

Defect pattern	Condition			Criteria
Line defect	Display of black, white, red, green, blue			0 line
Bright dots Note 2,Note 3	R+G+B			≤ 1dots
Dark dots Note 2 Note 4	R+G+B			≤ 4 dots
	Close defect dots Note 6	10mm≤D Note 5		Allowed
	Linked defect dots Note 7	D=0mm Note 5	2 defect dots	≤ 1 set
			3 defect dots or more	0 set
Total	Bright dots+Dark dots			≤ 5dots

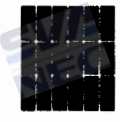
Note1: Inspection conditions are as follows.

Temperature	25±5℃
Inspection viewing distance	30±10cm(The distance between the inspector's eye and screen)
Inspection direction	0°≤θR≤20°, 0°≤θL≤20°
	0°≤θU≤20°
Inspection illumination	60±10 lux (at a display surface)

Note2: Dots which defect area is over the half of a dot (sub pixel) are defined as dot defect.
(for example)



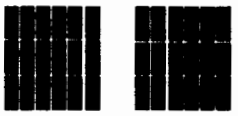
Dot defect



Not dot defect

Note3: Bright dots check patterns are full back pattern and 52/256 gray-scale black-white full screen pattern. Under these patterns ,the bright dots are easy to be determined, or these can't be taken as bright dots. (also refer to the limited samples)
(for example)

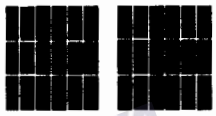
Bright dot defect



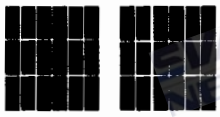
Not bright dot defect

Note4： Dark dots check patterns are full red, full green, full blue, and full white pattern. The dark dots are easy to be determined, or these can't be taken as dark dots. （also refer to the limited samples）

（ for example）



Dark dot defect



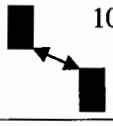
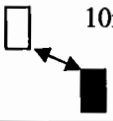
Not dark dot defect

Note 5： **D** is the distance between defect dots.

Note 6： See**"4.13.2 Close defect dots".**

Note 7： See**"4.13.3 Linked defect dots".**

4.13.2 Close defect dots

Defect pattern	: Bright dot : Dark dot	Criteria
Dark dots	 10mm ≤D	Allowed
Combinations between bright dot and dark dot	 10mm ≤D	Not counted

4.13.3 Linked defect dots

Defect pattern	: Bright dot : Dark dot	Criteria
2 defect dots		≤1 set
		Not counted

4.13.4 Appearance specifications

Defect pattern		Condition Note 1		Criteria
Impure ingredient Stains Dust	Dot shape	d<0.2mm		Allowed
		0.2mm≤d<0.3mm		≤10 points
		0.3mm≤d≤0.5mm		≤3 points
		d>0.5mm		0 point
		Adjacent other objects		
	Line shape	W<0.05mm		Allowed
		0.05mm≤W≤0.1mm	L<0.7mm	
			0.7mm≤L≤1.0mm	≤4 points
			L>1.0mm	0 point
		W>0.1mm		
Bubbles, Wrinkles, Dent		d≤0.2mm		Allowed
		0.2mm<d≤0.5mm		≤2 points
		d>0.5mm		0 point
Polarizer scratch		S≤0.2mm^2		Allowed
		S>0.2mm^2		0 point
Flick		Refer to limited samples		
Mura		Refer to limited samples		
Crosstalk		Refer to limited samples		

Note1: Definition of symbols is as follows.

d: Average diameter

(This diameter is the average length of a long axis and a short axis in each defect pattern.)

W: Width, L: Length, S: Area

Note2: Inspection conditions are as follows.

Temperature	25±5℃
Inspection viewing distance	30±10cm (The distance between the inspector's eye and screen.)
Inspection direction	0° ≤θR≤45°, 0° ≤θL≤45°
	0° ≤θU≤45°, 0° ≤θD≤45°
Illumination	700 lux (at an inspection desk surface)

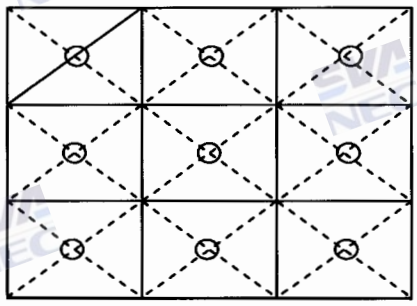
Note3: If any problems arise with the LCMS suppliers by suppliers, the custom and supplier will cooperate and make efforts to solve it with mutual confidence and respect.

5. RELIABILITY TESTS

Test items		Condition
High temperature and humidity(Operation)		① 60±2℃,RH=60%,240hours ② Normal temperature and humidity,1~24hours **Note1**
Heat cycle (Operation)		① 0±3℃...1hour 55±3℃...1hour ② 50cycles,4hours/cycle **Note1**
Thermal shock (Non operation)		① -20±3℃...30minutes 60±3℃ ...30minutes ② 100cycles,1hour/cycle ③ Temperature transition time is within 5 minutes.
ESD (operation)		① 150Pf,150Ω,±10kV ② 9 places on a panel surface ③10 times each place at 1 sec interval **Note2**
Dust (operation)		① Sample dust: No.15(byJIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval
Vibration (Non operation)		① 5-100Hz， acceleration of 11.76m/S^2 ② 1 minutes/cycle ③ X,Y,Z direction ④ 10 times each direction
Mechanical shock (Non operation)		① 294m/S^2， 11ms ②±X，±Y，±Z direction ③ 3 times each direction
Low pressure	operation	①53.3kPa (Equivalent to altitude 4,850m） ② 0℃±3℃...24hours ③ 55℃±3℃...24hours
	non-operation	① 15kPa (Equivalent to altitude 13,600m） ② -20℃±3℃...24hours ③ 60℃±3℃... 24hours

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points.



6. ESTIMATED LUMINANCE LIFETIME

	Luminance lifetime Note2		
	Module		Cold cathode Fluorescent lamp, Note3
Temperature	Ambient temperature of the product	55 ℃(Surface temperature at screen center)	Ambient temperature of the product
Condition	Continuous operation Luminance to maximum and IBL=5.0mArms/lamp	Continuous operation Luminance to maximum and IBL=5.0mArms/lamp	Continuous operation Luminance to maximum and IBL=5.0mArms/lamp
Luminance lifetime(MTTF) Note1	TBD	TBD	50,000 h
Definition of lifetime	The luminance lifetime is the time from initial luminance to half-luminance.		

Note1: This lifetime is the estimated value, and is not guarantee value.

Note2: This lifetime changes greatly with the ambient temperature. In case the product works in low-temperature environment, the lifetime becomes short remarkably.

Note3: This is reference data. This is the CCFL lifetime, not the lifetime of LCD module.

7. PRECAUTIONS

7.1 MEANING OF CUTION SIGNS

The following caution signs have very important meaning .**Be sure to read "10.2 CAUTIONS" and "10.3 ATTENTIONS", after understanding these contents!**

This sign have the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.

This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

7.2 CAUTIONS

touch lamp cables while turn on .Customers will be in danger of an electric shock

*** Do not touch the working backlight and IC. Customers will be in danger of burn injury.**

*** Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass.(shock :To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N)**

7.3 ATTENTIONS 

7.3.1 Handling of the product

① Take hold of both ends without touch the circuit board when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.

② Do not hook cables nor pull connection cables such as flexible cable and so on , for fear of damage.

③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.

④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deal with the product, because products may be damaged by electrostatic.

⑤The torque for mounting screws must never exceed 0.34N-m. Higher torque values might result in distortion of the bezel.

⑥The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings).And do not add undue stress to any portion (such as bezel flat area) except mounting hole portion. Bends or twist described above and undue stress to any portion except mounting hole portion may cause display

un-uniformity.

⑦Do not press or rub on the sensitive display surface .If customer clean on the panel surface, SVA-NEC recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.

⑧ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

⑨ Do not bend or unbend the lamp cable at the near part of the lamp holding rubber, to avoid the damage for high voltage side of the lamp. This damage may cause a lamp breaking and abnormal operation of high voltage circuit.

7.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.

② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environment temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)

③ Do not operate in a high magnetic field .Circuit boards may be broken down by it.

④ This product is not designed as radiation hardened.

⑤ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

7.3.3 Characteristics

The following items are neither defects nor failures.

① Response time, luminance and color may be changed by ambient temperature.

②The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.

③Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time ,and especially low temperature, because the LCD has cold cathode fluorescent lamps.

④Do not display the fixed pattern for a long time because it may cause image sticking .Use a screen saver, if the fixed pattern is displayed on the screen.

⑤The display color may be changed by viewing angle because of the use of condenser sheet in the backlight.

⑥Optical characteristics may be changed by input signal timings.

⑦The interference noise of input signal frequency for this product and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise doses not appear.

7.3.4 Other

①All GND and VCC terminals should be used without a non-connected line.

②Do not disassemble a product or adjust volume without permission of SVA-NEC.

③See "REPLACEMENT MANUAL FOR LAMPHOLDER SET", if customer would like to replace backlight lamps.

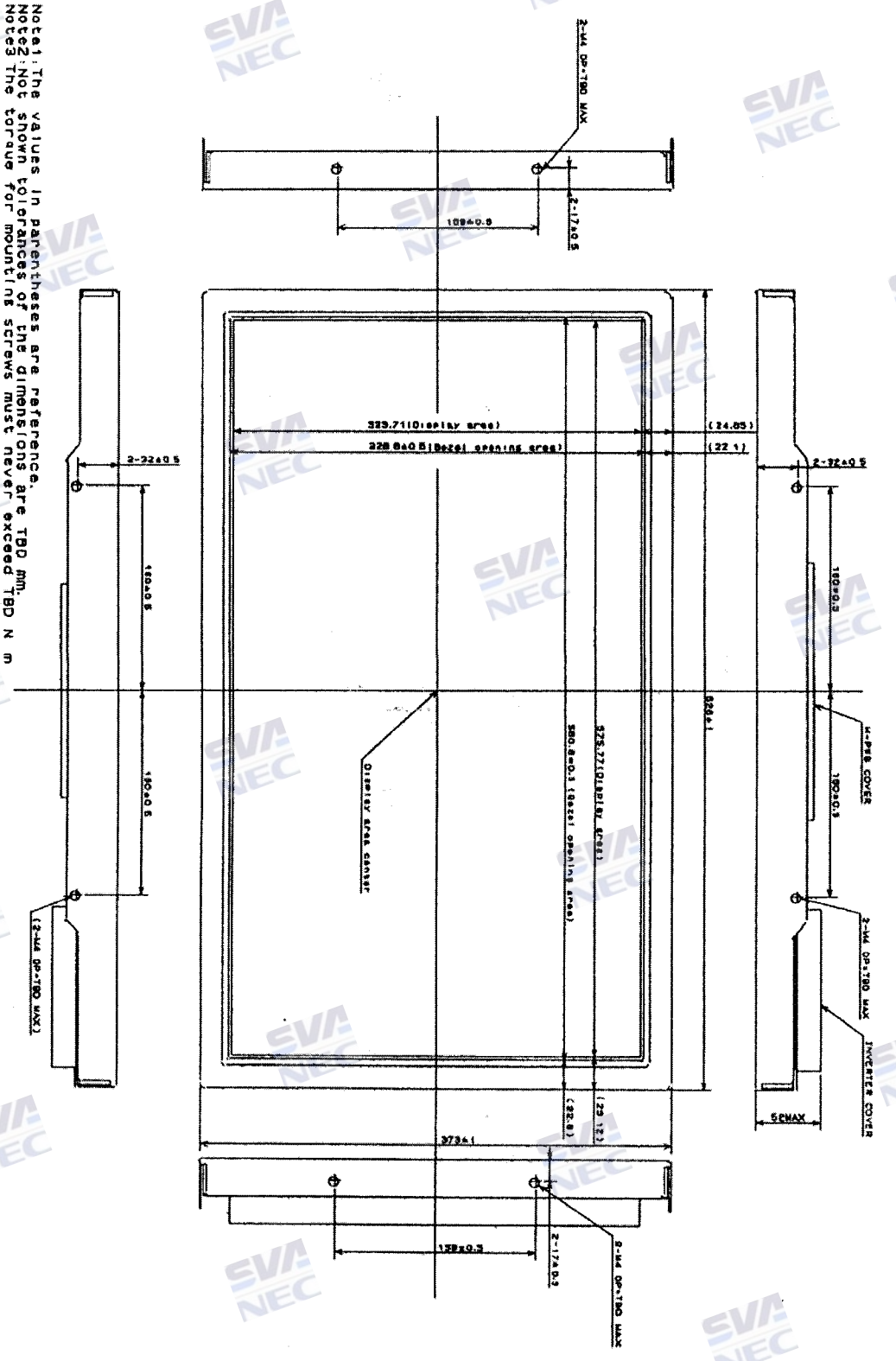
④Pay attention not to insert waste materials inside of products, if customer uses screw nails.

⑤Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to SVA-NEC for repair and so on .

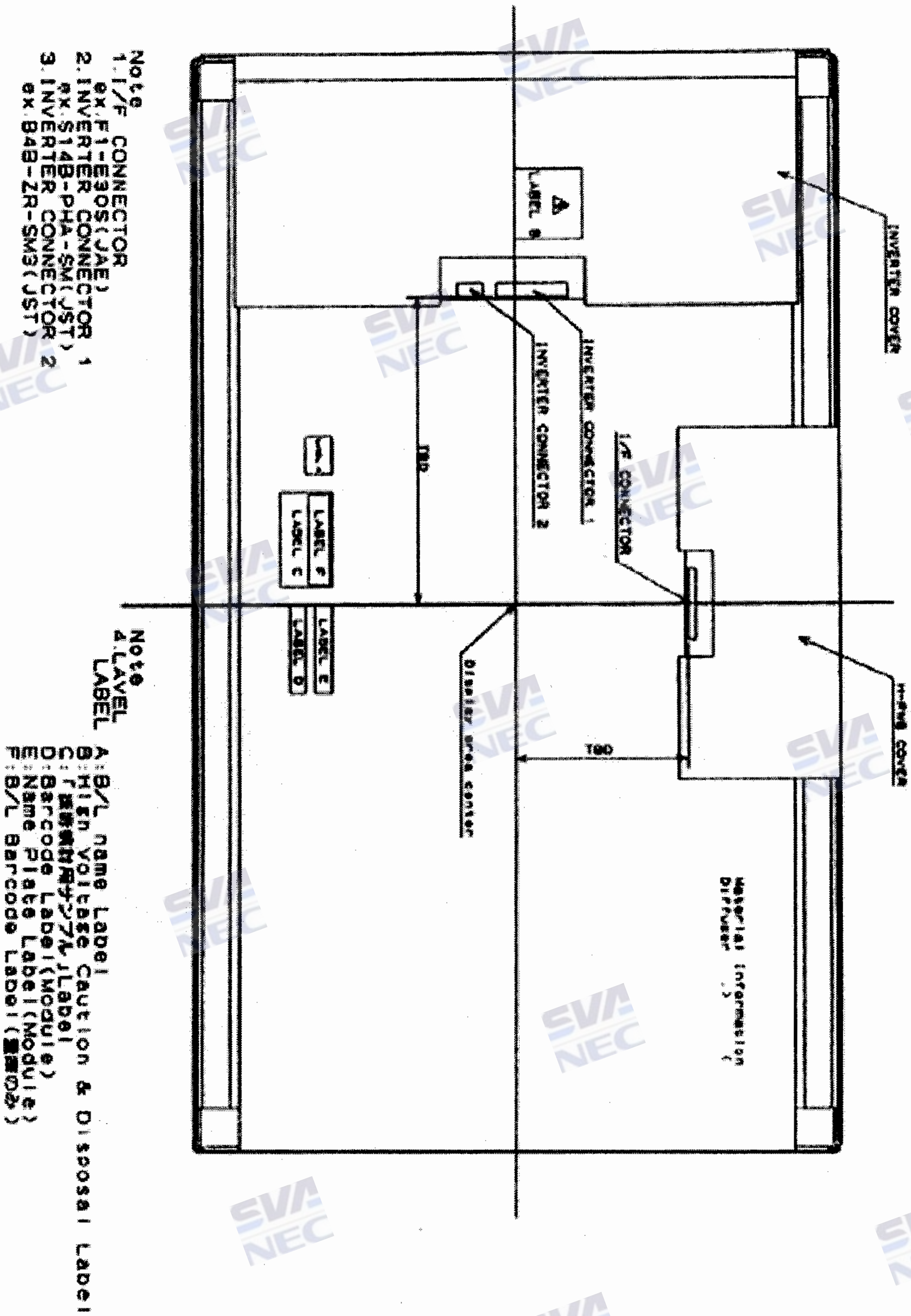
⑥Not only the module but also the equipment should be packed and transported as the module. becomes vertical .Otherwise, there is the fear that a display dignity decreases by an impact or vibrations.

8. MODULE OUTLINE

8.1 FRONT VIEW



8.2 BACK VIEW



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